Customer No.: 31561
Application No.: 10/711,574
Docket NO.: 13504-US-PA

REMARKS

Present Status of the Application

The drawings are objected to because there is no layer 228b in Fig. 5C. The Office Action rejected claims 1 and 10 because of lacking clear antecedent basis. The Office Action also rejected claims 3, 4, 5, 7, 12, 14 because a limitation invokes 35 U.S.C 112 6th paragraph by using the phase "means or step".

Applicant has amended paragraph [0047] of the specification to more clearly illustrate the embodiment of the invention. Fig. 5D is a cross-sectional view along line I-I' in Fig. 2 showing one of the steps of fabricating a dynamic random access. The layer 228b is not shown in Fig. 5D because it does not locate at the position along line I-I'.

Applicant has amended claims 1 and 10.

In claim 1,"the bottom portion" is amended to "a bottom portion"; "the interior surface" is amended to "an interior surface"; "the sidewall" is amended to "a sidewall"; and "the exposed semiconductor strip" is amended to "an exposed semiconductor strip".

In claim 10, "the exposed semiconductor strip" is amended to "an exposed semiconductor strip". However, the "conductive layer" in claim 10 does not lack an antecedent basis.

Claim 10. (currently amended) A method of fabricating a dynamic random access memory cell, comprising the steps of:

providing a substrate having a patterned mask layer thereon and a deep trench capacitor therein, wherein the deep trench capacitor comprises a lower electrode, an upper

electrode, a capacitor dielectric layer and a collar oxide layer, and the patterned mask layer exposes the upper electrode;

forming a trench in the substrate on one side of the deep trench capacitor, wherein the trench exposes a portion of the substrate and the upper electrode;

depositing a semiconductor material layer into the trench;

patterning the semiconductor material layer to form a semiconductor strip and two openings exposing the substrate, wherein one end of the semiconductor strip is positioned next to the upper electrode while the other end of the semiconductor strip is positioned next to the substrate;

forming a gate dielectric layer over the substrate to cover ~~the~~ an exposed semiconductor strip and the substrate; and

forming ***a conductive layer*** over the gate dielectric layer, wherein ***the conductive layer*** crosses over the semiconductor strip, and the semiconductor strip covered by the conductive layer serves as a channel region.

Applicant has amended a typographic error in claim 3. That is, "the step for" is amended to "the step of".

The "step of" in claims 3, 4, 5, 7, 12 and 14 does not invoke 35 U.S.C 112 6th paragraph. Any element in a claim that does not explicitly state "means for" performing a specific function, or "step for" performing a specific function, is not to be interpreted as a "means" or "step" clause as specified in 35 U.S.C 112, 6th paragraph. In particular, the use of "step of" in the claims herein is not intended into invoke the provisions of 35 U.S.C. 112, 6th paragraph.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-17 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,

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